

Partial Reconfiguration

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Abstract

With the release of ISE 12.1 partial reconfiguration have left the realm of academic curiosity to become a fully supported design flow with applications ranging from medical to aerospace fields. In this tutorial we will review the evolution of the idea of reconfigurable hardware and the tools that made it finally possible. The tutorial will also enumerate the differences between the latest beta PR tools and the newly released commercial version of the tool. A short on-line demonstration of the tools flow will be done to provide the students with a feel for the complexities of the tool and the potential of the design flow.

Biography

Dr. Vera received his bachelor degree from the Pontifical University of Peru, and his masters and PhD degrees from the University of New Mexico in 1998, 2004 and 2008 respectively. He joined Micro-RDC on May 2008 where he currently is researching alternative methods for radiation mitigation on field programmable gate arrays. He is also a research professor with the University of New Mexico.

While in grad school, Dr. Vera worked as a research assistant for different projects mainly related to FPGA's partial reconfiguration capabilities. He developed new design flows to allow dynamic partial reconfiguration in his PhD dissertation and published several papers on dose upset investigations for different Xilinx devices. He also obtained two internships with the Mathematical and Modeling and Analysis group at Los Alamos National Laboratory. During his time at LANL he performed research on novel numerical optimization methods. He also held research assistantships in projects with Xilinx and the Air Force Research Laboratory, where he acquired experience on design, testing and implementation of hardware systems based on field programmable gate arrays. Since his dissertation work, partial reconfiguration has remained one of Dr. Vera's main research interests.