

# **Designing FPGAs for Space – Top Down, Bottom Up, Inside Out, Etc.**

Mr. Chris Dailey

## **Bio:**

Christopher Dailey is a computer engineer for NASA's Goddard Space Flight Center with over 20 years of experience in digital design of spacecraft and ground-based FPGAs, ASICs, boards, boxes and systems. Since 2002, he has co-designed and/or reviewed FPGAs for several space programs including the James Webb Space Telescope (JWST), Magnetosphere Multiscale Mission (MMS), Solar Dynamics Observatory (SDO) Lunar Reconnaissance Orbiter (LRO) and Gamma-Ray Large Area Space Telescope (GLAST). He has been heavily involved in developing robust SpaceWire networks, routers and nodes, including enhancements to the SpaceWire standard. He received a B.S. in Computer Engineering from The Pennsylvania State University in 1991.

## **Tutorial Description:**

Due to the increasingly significant and complex roles FPGAs serve in spacecraft, the cost of spacecraft and the challenges of space environments, developing FPGAs for space applications necessitates proving designs not only meet their functional and performance requirements but are robust enough to work throughout their mission, properly responding to radiation upsets and long-term electrical changes. This tutorial will describe a typical top-down design approach but focus on using many different ways to verify designs, discussing pros and cons of each.