

## Programming FPGA Using ROCCC

A Half-Day Tutorial Proposal for ReSpace/MAPLD 2010 - Topic: Reconfigurable Computing

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### ABSTRACT

ROCCC (Riverside Optimizing Compiler for Configurable Computing) is a C to VHDL compilation framework specifically focused on FPGA-based code acceleration. Its focus is on compile time transformations and optimizations aimed at generating an efficient circuit from a loop nest. Its objectives are to maximize parallelism within the constraints of the target device, optimize clock cycle time by efficient pipelining and minimize the area utilized. Furthermore, ROCCC relies on extensive and unique loop analysis techniques to increase the reuse of data fetched from off-chip memory. ROCCC 2.0 is a free and open source tool that supports a modular bottom-up approach to the programming of FPGA accelerators, supporting code reuse at multiple levels while maintaining full compatibility with C. It has been ported to several platforms including Xilinx development boards and the Convey Computers HC-1.

### CONTACT INFORMATION

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### Detailed Description

**Tutorial Goals:** The tutorial will also cover the motivations, problems, and potentials of the even more difficult task of designing hardware accelerators from high level languages. The Riverside Optimizing Compiler for Configurable Computing (ROCCC) will be presented as an integral part of a working design flow for the creation of hardware accelerators from C. A detailed description of both the internals and interface of the ROCCC compiler will be presented. All of the novel features of ROCCC will be demonstrated and the motivations and usage will be discussed.

**General Description:** The tutorial material will cover the advancements made with the ROCCC 2.0 compiler. Unlike similar tools designed for high-level synthesis, ROCCC does not support the generation of arbitrary hardware circuits. Rather, its focus is on compile time transformations and optimizations aimed at generating an efficient circuit from a loop nest. Analysis of what types of applications are appropriate for hardware accelerators and which are best suited for CPUs will be addressed.

ROCCC's objectives are to maximize parallelism within the constraints of the target device, optimize clock cycle time by efficient pipelining and minimize the area utilized. Furthermore, ROCCC relies on extensive and unique loop analysis techniques to increase the reuse of data fetched from off-chip memory. The specific optimizations necessary for creating an efficient circuit as well as control of those optimizations will be discussed and explained. Both high level and low level optimizations can be controlled by the user, and the drastic effect of these optimizations will be demonstrated.

One of the key factors in hardware development is reusability. ROCCC supports reusability through the use of *modules*, which correspond to basic hardware blocks. These modules can be used in the creation of larger modules and *systems*. Modules are integrated directly into the pipelined hardware that is created by ROCCC, all without ever leaving the C level. Examples of building larger systems from small modules will be shown in C and compared with HDL-based solutions.

For the demonstration of ROCCC, various high level examples in C will be shown and described and then compiled into hardware. The resulting hardware will be shown in a simulation environment or running on an FPGA. The ROCCC distribution and GUI will be demonstrated on the same machine that the presentation is made on, no additional equipment will be necessary.

## **SHORT VITAE WALID NAJJAR**

### **A. Education**

- Ph.D. in Computer Engineering (August 1988), University of Southern California.
- M.S. in Computer Engineering (June 1985), University of Southern California.
- B.E. in Electrical Engineering (July 1979), American University of Beirut, Lebanon.

### **B. Experience**

- Professor/Associate Professor, University of California Riverside, Computer Science & Engineering, (2000 – present)
- Associate/Assistant Professor, Colorado State University, Dept. of Computer Science, (1989 – 2000).
- Computer Scientist, USC/Information Sciences Institute, Marina del Rey, CA (88-89).

### **C. Honors And Awards**

- Elected Fellow AAAS, 2009.
- Elected Fellow of the IEEE, 2007.

### **D. Past Tutorials and Short Courses**

- Opportunities and Challenges of Reconfigurable Computing, Department of Computer Engineering, University of Siena, Siena, Italy, February 2010 (4 days).
- Programming FPGA-Based Accelerators using ROCCC 2.0, High-Performance and Embedded Architectures and Compilers, Pisa, January 25, 2010 (with Jason Villarreal) (Half day).
- Programming FPGA-Based Accelerators using ROCCC 2.0, U. Politecnica de Catalonia and Barcelona Supercomputer Center, January 20, 2010 (with Jason Villarreal) (2 days).
- Opportunities and Challenges of Reconfigurable Computing. ACACES 2009, 5th International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES, a HiPEAC event), July 12 to July 18, 2009 Terrassa, Spain, (one week).
- Reconfigurable computing -- platforms, compilation and applications. Half-day tutorial at the IEEE/ACM Int. Symp. on Microarchitecture (MICRO), Dec. 2007, Chicago, IL (with F. Kurdahi) (Half day).
- Compiling Code Accelerators for FPGAs. Half-day tutorial at the IEEE/ACM Int. Conf. on Compiler, Architecture and Synthesis for Embedded Systems (CASES), part of ESWEEK, October 2007, Salzburg, Austria (Half day).

### **E. Recent Relevant Publications**

- Moussalli, M. Salloum, W. Najjar and V. Tsotras. Accelerating XML Query Matching Through Custom Stack Generation on FPGAs, Proc. Int. Conf. on High-Performance Embedded Architectures and Compilers, January 25-27, 2010, Pisa, Italy.
- W. Najjar and J. Villarreal. Modular Design of FPGA-Based Accelerators in C, Military and Aerospace Programmable Logic Devices (MAPLD), NASA Goddard Space Flight Center, Greenbelt, MD, August 2009.
- A. Mitra, M. Vieira, P. Bakalov, W. Najjar, V. Tsotras, Boosting XML filtering through a scalable FPGA-based architecture, in Fifth Biennial Conference on Innovative Data Systems Research (CIDR), January 2009, Pacific Grove, CA, USA.
- J. Villarreal and W. Najjar. [Compiled Hardware Acceleration of Molecular Dynamics Code](#), in Int. Conf. on Field Programmable Logic and Applications (FPL'08), Heidelberg, Germany, September 2008.
- A. B. Buyukkur and W. Najjar. [Compiler Generated Systolic Arrays For Wavefront Algorithm Acceleration on FPGAs](#), in Int. Conf. on Field Programmable Logic and Applications (FPL'08), Heidelberg, Germany, September 2008.
- Z. Guo, W. Najjar, A. B. Buyukkur. [Efficient Hardware Code Generation for FPGAs](#), to appear in ACM Transactions on Architecture and Compiler Optimizations (TACO), ACM.

- Mitra, W, Najjar, L. Bhuyan. [Compiling PCRE to FPGA for Accelerating SNORT IDS](#), in the ACM/IEEE Symposium on Architecture for Networking and Communication Systems (ANCS), Orlando, FL, Dec. 2007.
- M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Prichard, P. Palazzari and G. Kuzmanov. [OpenFPGA CoreLib Core Library Interoperability Effort](#), in Parallel Computing, Vol. 34, No. 4, pp. 231-244, Elsevier.
- Z. Guo, A. B. Buyukkurt, J. Cortes, A. Mitra, W. Najjar. [A Compiler Intermediate Representation for Reconfigurable Fabrics](#) in International Journal of Parallel Programming (IJPP), Springer.
- K. Schleupen, S. Lekuch, R. Mannion, Z. Guo, W. Najjar and F. Vahid. Dynamic Partial FPGA Reconfiguration in a Prototype Microprocessor System, in Int. Conf. on Field Programmable Logic (FPL) Amsterdam, The Netherlands, August 2007.

## **SHORT VITAE JASON VILLARREAL**

### **A. Education**

- Ph.D. in Computer Science (August 2008), University of California, Riverside.
- B.S. in Computer Science (July 1998), University of California, Riverside.

### **B. Experience**

- Senior Engineer, Jacquard Computing (2009-present).
- Post-Doctoral Researcher, University of California, Riverside (2008-2009).
- Lecturer, University of California, Riverside (1999-2006).

### **C. Past Tutorials and Short Courses**

- Programming FPGA-Based Accelerators using ROCCC 2.0, High-Performance and Embedded Architectures and Compilers, Pisa, January 25, 2010 (with Walid Najjar) (Half day).
- Programming FPGA-Based Accelerators using ROCCC 2.0, U. Politecnica de Catalonia and Barcelona Supercomputer Center, January 20, 2010 (with Walid Najjar) (2 days).

### **D. Publications**

- J. Villarreal, A. Park, W. Najjar and R. Halstead. Designing Modular Hardware Accelerators in C with ROCCC 2.0, Field Programmable Custom Computing Machines (FCCM), 2010.
- W. Najjar and J. Villarreal. Modular Design of FPGA-Based Accelerators in C, Military and Aerospace Programmable Logic Devices (MAPLD), NASA Goddard Space Flight Center, Greenbelt, MD, August 2009.
- J. Villarreal and W. Najjar. [Compiled Hardware Acceleration of Molecular Dynamics Code](#), in Int. Conf. on Field Programmable Logic and Applications (FPL'08), Heidelberg, Germany, September 2008.
- G. Stitt and J. Villarreal. Recursion Flattening. Great Lakes Symposium on Very Large System Integration (GLVLSI), 2008.
- J. Villarreal, J. Cortes, and W. Najjar. Compiled Code Acceleration of NAMD on FPGAs. Reconfigurable Systems Summer Institute (RSSI), 2007.