

Optimizing Mitigation Strategies for FPGA Critical Applications

Ms. Melanie Berg



Melanie Berg received her MS degree in Electrical Engineering from the University of Pittsburgh in 1990. In 1988, during her graduate studies, Ms. Berg combined her expertise in chip placement and design methodology by creating optimized VHDL modules for Digital Systems of Pittsburgh PA. In 1990 Ms. Berg joined IBM's ASIC Advanced Logic Design Team in Poughkeepsie, NY. She has been part of several development teams responsible for high speed multi-million gate ASIC and complex FPGA implementations. Later in her career at Ball Aerospace, Ms. Berg was an FPGA designer and instructor for various space-flight projects. Ms. Berg is currently a member of IEEE and has joined the Radiation Effects and Analysis group at NASA Goddard Space Flight Center. She has published and presented several papers concerning such topics as Reliable Synchronous Design Methodology, Mitigation Strategies for Critical Circuitry, and Hardness Assurance for Space Flight Projects. Ms. Berg is presently investigating radiation effects and applicable mitigation strategies for the potential insertion of Field Programmable Gate Arrays (FPGAs) and ASICS into critical space flight projects.

Course Summary:

The course "Optimizing Mitigation Strategies for FPGA Critical Applications" will begin with a description of radiation effects in FPGA devices. This section will explain the various types of upsets that can occur due to ionizing particles per FPGA type. Newly obtained up-to-date radiation data for Actel RTAXs, Actel ProASIC3E, and the Xilinx Virtex series will be provided.

A summary of mitigation strategies will follow the radiation effects segment. Modes of mitigation failure (the untold story) will also be discussed. Material regarding failure and success scenarios will be justified within the presentation by radiation data, simulations, timing diagrams, truth tables, and common sense... a designer's haven.

The course will conclude with a guideline on how to combine the FPGA radiation characterization data with selected mitigation schemes to determine design driven upset rates.

Attendees will gain practical information and design strategies for critical aerospace and military projects.

Key words: anti-fuse FPGA configuration, flash-based FPGA configuration, SRAM-based FPGA configuration, Triple Modular Redundancy (TMR), Temporal Redundancy (TR), Dual Redundancy (DR), scrubbing, re-configuring, safe-state-machines, watchdogs, detection, recovery, and error-rate prediction.