

Thursday (11/4/10)

7:30 am	Track 1 – ReSpace Session IV - On The Horizon	Breakfast
8:30 am – 8:50 am		CANopen Networks As An Enabler For Modern Space-Borne Control Systems: The European Space Agency’s Perspective – Gianluca Furano - European Space Agency (ESA)
8:50 am – 9:10 am		Composing Video/Sensor-Based Automated Notification Systems Using Spatial Programming: Frank Vahid – University Of California
9:10 am – 9:30 am		MONOLITHIC-MCM ANALOG IC DESIGN FOR SPACE: Reid Wender- Triad Semiconductor, Inc.
9:30 am – 10:00 am		Psoc: Walt Anderson – SNC Space Systems
10:00 am – 10:30 am		Break
10:30 am – 10:50 am		QuickSAT and the step_SATdb database, a web based and open source concurrent satellite design automation environment: Andrew Santangelo - sci_Zone, Inc.
10:50 am – 11:10 am		Adaptive Wiring Manifold: Marios Pattichis – University Of New Mexico
11:10 am – 11:30 am		A Virus-Based Transistor For Integrated Molecular-Scale Circuits: Ashwani K. Sharma – AFRL/RVSE
11:50 am		Lunch, Closing

Thursday (11/4/10) contd...

7:30 am	Track 2 – MAPLD Session D – Designing With FPGAs And PLDs	Breakfast
8:30 am – 8:50 am		Implementing SpaceWire Routers As Standard Products using FPGA Technology: Sandi Habinc, Daniel Hellström, Kristoffer Glembo - Aeroflex Gaisler
8:50 am – 9:10 am		Dynamic Partial Reconfiguration Of Softcore Processors On The Virtex 5: Mike Wirthlin, Michael Wirthlin, Jonathon Donaldson, Jeffrey Kalb - Brigham Young University, Sandia National Laboratories
9:10 am – 9:30 am		FPGA SynthesisBased Radiation Effects Mitigation Using Triple Modular Redundancy And Safe FSM Implementations: Daniel Platzker - Mentor Graphics Corporation
9:30 am – 9:50 am		Radiation Hardening By Software For The Embedded PowerPC, Preliminary Findings: John Paul Walters, Mark Bucciero, Matthew French - University of Southern California, Information Sciences Institute
9:50 am – 10:10 am		Actel RTAX-DSP Design Techniques For High Reliability Application: Minh Nguyen - Actel Corporation
10:10 am – 10:30 am		Break
10:30 am – 10:50 am		Applying Modern Verification Methods To VHDL Designs: Doug Smith - Doulos-Developing Design Know-How
10:50 am – 11:10 am		Design Choices And Guidelines For Configuration Monitoring And Management Of The RHBD Virtex-5QV Space-Grade FPGA: Y.C. Wang, Gary Swift, Chenwei Tseng – Xilinx Corp.
11:10 am – 11:30 am		Prototyping V-5QV Space Applications Using The Commercial-Grade FPGAs And Boards: Gary Swift, Carl Carmichael – Xilinx Corp.
11:30 am – 11:50 am		A Design Flow For FPGA Conversion Into Radiation-Hardened ASIC: Ran Ginosar, Tuvia Liran, Dov Alon - Ramon-Chips Ltd.
11:50 am		Lunch, Closing